A Design Way of High Frame Frequency Image Acquisition and Transmission System

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Abstract. There is a problem of existing vast information at high frame frequency image acquisition and transmission system, which will generate a result that real-time performance of image acquisition and transmission system is not well. The article propose a new scheme of high frame frequency image real-time acquisition and transmission way, it uses the medium configuration mode that it transmits concurrently 4 pixel data , clock signal and control signal to solve the problem of the above, by means of studying the vast data of the image acquisition and transmission. For the high speed real-time video image of resolution of 1280*1024, a frame rate 400f/s and the width of 8bit, the experiment result show that the system can complete the acquisition and transmission of high frame frequency image effectively.

1 Introduction

Digital image processing is widely used in military technology, scientific research, industrial production and other fields. High frame rate image acquisition can reflect the motion process of research of object very well, from which we can get valuable information[1], but there is a problem that it exist large amount of data transmission and real-time acquisition. For the video image which the resolution of 1280×1024 frame rate of 300f/s and width 8bit, it requires to process an image in 3.3ms,including video signal synchronization, sampling, digitization, transmission and real-time acquisition, this is difficult to achieve for high resolution image[2].

Compared to conventional PCI capture card interface, High frame rate digital image real-time acquisition and display system base on Camera Link interface, reduce costs, save space and aim to ensure the stability of the system work. Camera Link is a communication interface for vision application to provide a specification, which extends the base technology of Channel Link. The Camera Link that in the conventional LVDS (Low Voltage Differential Signaling)data transmission on the basis of which loads a parallel turn serial transmitter and a serial turn parallel receivers, uses SER / DES technology, data transfer rate up to 4.8Gb/s. It can effectively solve the video data speed matching between the output and collection problems.

2 High-speed Video Images in Real-time Acquisition System

High speed video image acquisition system consists of two parts, one is image photoelectric conversion module, and the other is image processing module. The first part is the conversion module of optics and electrics. In the high frame rate camera, an optical signal by the CMOS camera image sensor is converted to an analog electrical signal converted by the A / D conversion circuit into a digital signal. The digital signals that output by CMOS camera is converted by Channel Link encode chip in the Peripheral circuits to analog LVDS signal which is in line with the Camera Link standard. The second part is the image processing module. The LVDS signals that channel link decoder chip received is converted to LVTTL parallel digital signal, and then input the signals to FPGA chip. Finally, through VGA controller module, FPGA chip are displaying the video image on the LCD monitor.

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3 Circuit Design of High Speed Video Image Acquisition System

3.1 Video Image Transmission Module

The Camera Link standard is developed by several industrial-grade cameras and capture card manufacturers. The interface has commonality, and interface standard specifies the pin assignment and the corresponding connector specification, to ensure compatible device interfaces to seamless connection.

The Channel Link standard specifies the transmission of image data using LVDS technology. LVDS signal is a low voltage swing transmission technology that is in accordance with differential level standard. The Signal through the 350mA constant current source drives, Transmission approximately 350mV low voltage differential signal over the equilibrium line. At the same time, the clock frequency can reach 82MHz. The outside noise couples to the two differential signal lines, but the receiver are only interested in the difference between the transmitted signal and the received signal. Therefore, noise can be effectively suppressed. Due to LVDS has a small voltage swing, differential lines' data can be transmission on the relatively high rate. LVDS drivers and receivers also enables the hot-swap, constant current source driver can effectively prevent damage to the equipment. The Camera Link interface has three configurations: Basic configuration, Medium configuration, Full configuration. According to the high frame rate camera technical requirements, this design uses medium configuration which has eight LVDS video data channels, four camera control signal lines CC1, CC2, CC3, CC4 and two serial communications signals. During the 82MHz pixel clock, every clock cycle transmitted 8 pixels. So the amount of data transmitted per unit time is larger than high-speed video image that the resolution of 1280×1024, frame rate 300f / s and 8bit bit width.

The data is serialized 7:1, and the four data streams and a dedicated clock are driven over five LVDS pairs. The receiver accepts the four LVDS data streams and LVDS clock, and the drivers the 28 bits and a clock to the board. During one clock cycle, each LVDS signal output 7 bit data. About the 28 bits data, wherein the 24 bit data representing three-depth is eight pixels, the other 4 bit are representative frame signal (FVAL), effective signal (LVAL), the data valid signal (DVAL) and retention signal (Spare).

Camera Link video data signal has 8 ports that named Port A to Port H, and each individual port includes eight parallel bits. In the Medium configuration mode， Port A, Port B, Port C was assigned to drive a Camera Link / on the receiver， Port D, Port E, Port F is assigned to the second Camera Link driver / receiver， and every port outputs one pixel in one clock cycle. Therefore, in this configuration mode each clock cycle output 8 pixels.

There are four camera control signals,CC1 is used to external synchronization signal,CC2 is used to pixel reset,CC3is used to the forward signal,CC4 undefined.

Camera Link standard defines the other two pairs of LVDS cables to achieve control of asynchronous serial communication between the camera and the image acquisition module. Two pairs of serial signals were Ser TRG and Ser TC， they communication format conforms to the RS-232 protocol standard. Through the Ser TC pin, AVR control panel writes to the register parameters to configure the CMOS camera lens, in order to control the camera's clock frequency, exposure mode, gain mode, Tag mode, reading the area of interest and so on, and by the Ser TRG pin， reading the configuration parameter of the camera to verify that the configuration is correct. Serial transmission of data formats, including one start bit, eight data bits, one stop bit, no handshaking and parity.

3.2 Video Image Acquisition Module Design

This system uses BASLER company acA2000 series camera, the main chip is selected ALTERA EP4CGX150DF31 which has 149,760 logic cells, 720M9K memory modules, 8PLL and 360 multipliers, etc. As a core part of the whole data acquisition card, FPGA control module take charge of the camera data collection storage and serial configuration. Because of Camera Link interface‘s strict definition, Video image acquisition module that under the coordination between the clock

control and the timing of FVAL and LVAL valid signal complete the identification of valid data, by counting the pixel counter X and counter Y. then methodical store the data that acquisition one time.

In order to avoid extended adjuvant SDRAM memory in the FPGA chip, and prevent both a large number of circuit board wiring and complex memory management control logic, the system uses FPGA chip built-in hard IP core M9K of RAM for caching data. For the inconformity of the clock of the image acquisition and VGA displays, we use a single input single output port RAM. Each block RAM to store four pixels, we want to generate 80 identical ram blocks to store data.

When the LVAL signal is set, write to the collected data by the timing of pixel counter. After filling with one row, the row counter incremented one. The FVAL signal set high when filling with one frame image fully, then begin the second frame image acquisition. The process followed By Recycling. Figure 1 is Signal Tap captured waveforms.

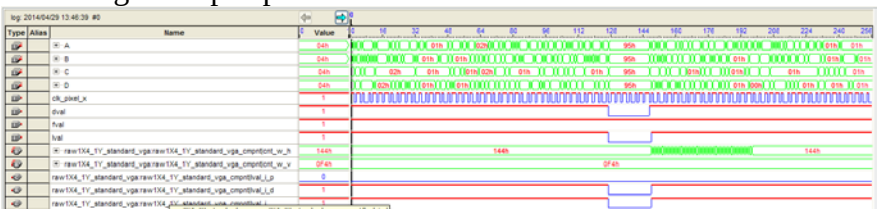

Figure 1:Key signal waveform of image acquisition

3.3 Design of Video Image Display Module

In order to effectively analyze and verify the captured high-speed image, we need to put the image displayed on the LCD monitor. Depending on the resolution and refresh rate, the display mode can be divided into: VGA (640*480) display, QVGA (320*240), XGA (800*600) .

VGA (Video Graphics Array) is IBM Company introduced a video transmission standard in the year of 1987, it has a high resolution, fast display rate, rich colors, etc. So it is widely used in the field of display. VGA uses the display style of progressive scan, which starts scanning from the upper left of the screen, from top to bottom. After scan one line, use lines synchronous signal synchronization and use Electron beam blanking to LCD, then make it back to the starting position of next line to the left of the screen. When finished scanning all rows, use frames synchronous signal synchronization, then return to the scanning start position of the top left of the screen, while for field blanking and ready to scan the next frame.

The key point is the VGA display timing generation module generates the required timing. If the timing has a little deviation, the display is abnormality. VESA has regulated the monitor's timing, for example: Horizontal and vertical sync pulse timing , Back porch b, Display interval c, Front porch d. the requirements of VGA industry standard display modes: horizontal sync and vertical sync are negative, that is to say the requirement of sync pulse is negative.

VGA display timing generator module provides the HS and VS signals, and set the resolution to 640 × 480, while providing the column address counter and the line counter generation module. According to the requirement of the VGA timing, address generator and RAM control module detect the row and column counter to extract the data. Then at a predetermined time to transfer the image data to the video D / A converter chip ADV7123, finally sent to the VGA interface in the LCD display[3].

4 System Performance Testing and Analysis

In order to test the performance of the system, the system design collection, record and display circuit, generate sequential control logic[4] by writing the Verilog HDL code.

So as to facilitate software debugging and shorten development time, using third-party software for the simulation of the system. Using signal tap II to observe internal signals of the FPGA chip. Real time acquisition sequence is shown in Figure 2. We know the design meet the requirements and stable operation for a long time no error frame[5-6].

On the premise of meet the technical index, the writer collects the dynamic target and then real-

time display image. Experiment results show that the image acquisition system can complete the acquisition and storage on the resolution of 1280×1024 300f/s, frame rate, bit width 8bit high speed video image[7].

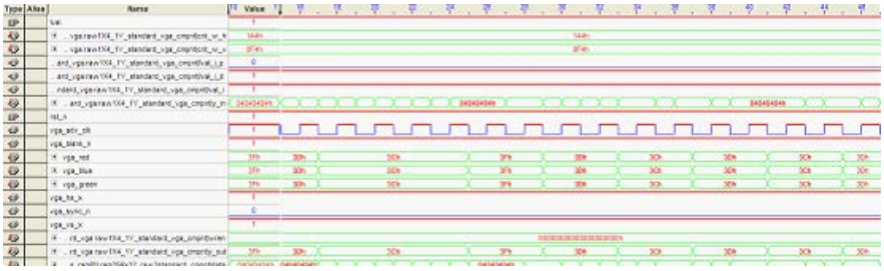

Figure 2:Real time acquisition timing diagram

5 Conclusions

This paper provides an effective solution about real-time high frame rate image acquisition system Camera based on Link for the acquisition, transmission and storage of high speed image data. In this paper, the Verilog HDL code has good versatility and portability, and generating logic control circuit in the FPGA chip to control image acquisition and RAM memory's read and writing. Experiments show that the system can complete resolution of 1280×1024, frame rate 300f/s, 8bit bit wide high-speed video image acquisition and storage. For the highly integrated, strong real-time, the system can provide a more intuitive analysis of experimental data information for the industrial inspection and scientific research.

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